


**PALM INTRANET**

Day : Sunday  
Date: 5/1/2005  
Time: 09:00:11

**Inventor Name Search Result**

Your Search was:

Last Name = LEE

First Name = JUNG-BAE

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">08771198</a>	<a href="#">5844438</a>	150	12/20/1996	CIRCUIT FOR GENERATING AN INTERNAL CLOCK FOR DATA OUTPUT BUFFERS IN A SYNCHRONOUS DRAM DEVICES	LEE, JUNG-BAE
<a href="#">08996192</a>	<a href="#">5920511</a>	150	12/22/1997	HIGH- SPEED DATA INPUT CIRCUIT FOR A SYNCHRONOUS MEMORY DEVICE	LEE, JUNG-BAE
<a href="#">08998326</a>	<a href="#">6018259</a>	150	12/24/1997	PHASE LOCKED DELAY CIRCUIT	LEE, JUNG-BAE
<a href="#">09044391</a>	<a href="#">6078546</a>	150	03/18/1998	SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE WITH DOUBLE DATA RATE SCHEME	LEE, JUNG-BAE
<a href="#">09049739</a>	<a href="#">6075384</a>	150	03/27/1998	CURRENT-MODE BIDIRECTIONAL INPUT/OUTPUT BUFFER	LEE, JUNG-BAE
<a href="#">09104152</a>	<a href="#">6130558</a>	150	06/23/1998	DATA TRANSFER CIRCUIT AND METHOD FOR A SEMICONDUCTOR MEMORY	LEE, JUNG-BAE
<a href="#">09136871</a>	<a href="#">6147527</a>	150	08/19/1998	INTERNAL CLOCK GENERATOR	LEE, JUNG-BAE
<a href="#">09168535</a>	<a href="#">6373913</a>	150	10/08/1998	INTERNAL CLOCK SIGNAL GENERATOR INCLUDING CIRCUIT FOR ACCURATELY SYNCHRONIZING INTERNAL CLOCK SIGNAL WITH EXTERNAL CLOCK SIGNAL	LEE, JUNG-BAE
<a href="#">09196994</a>	<a href="#">6232812</a>	150	11/20/1998	INTEGRATED CIRCUIT DELAY LINES HAVING PROGRAMMABLE AND PHASE MATCHING DELAY CHARACTERISTICS	LEE, JUNG-BAE

<u>09235471</u>	<u>6151271</u>	150	01/22/1999	INTEGRATED CIRCUIT MEMORY DEVICES HAVING DATA SELECTION CIRCUITS THEREIN WHICH ARE COMPATIBLE WITH SINGLE AND DUAL RATE MODE OPERATION AND METHODS OF OPERATING SAME	LEE, JUNG-BAE
<u>09318206</u>	<u>6222411</u>	150	05/25/1999	INTEGRATED CIRCUIT DEVICES HAVING SYNCHRONIZED SIGNAL GENERATORS THEREIN	LEE, JUNG-BAE
<u>09356269</u>	<u>6151272</u>	150	07/16/1999	INTEGRATED CIRCUIT MEMORY DEVICES THAT UTILIZE DATA MASKING TECHNIQUES TO FACILITATE TEST MODE ANALYSIS	LEE, JUNG-BAE
<u>09378099</u>	<u>6232797</u>	150	08/20/1999	INTEGRATED CIRCUIT DEVICES HAVING DATA BUFFER CONTROL CIRCUITRY THEREIN THAT ACCOUNTS FOR CLOCK IRREGULARITIES	LEE, JUNG-BAE
<u>09409178</u>	<u>6154416</u>	150	09/30/1999	COLUMN ADDRESS DECODER FOR TWO BIT PREFETCH OF SEMICONDUCTOR MEMORY DEVICE AND DECODING METHOD THEREOF	LEE, JUNG-BAE
<u>09498858</u>	<u>6188631</u>	150	02/07/2000	SEMICONDUCTOR MEMORY DEVICE COLUMN SELECT CIRCUIT AND METHOD FOR MINIMIZING LOAD TO DATA INPUT/OUTPUT LINES	LEE, JUNG-BAE
<u>09518144</u>	<u>6262938</u>	150	03/03/2000	SYNCHRONOUS DRAM HAVING POSTED CAS LATENCY AND METHOD FOR CONTROLLING CAS LATENCY	LEE, JUNG-BAE
<u>09524037</u>	<u>6240039</u>	150	03/13/2000	SEMICONDUCTOR MEMORY DEVICE AND DRIVING SIGNAL GENERATOR THEREFOR	LEE, JUNG-BAE
<u>09542042</u>	Not Issued	061	03/31/2000	HIGH FREQUENCY EQUALIZER USING A DEMULTIPLEXING TECHNIQUE AND RELATED SEMICONDUCTOR DEVICE	LEE, JUNG-BAE

<u>09543759</u>	<u>6337809</u>	150	04/05/2000	SEMICONDUCTOR MEMORY DEVICE CAPABLE OF IMPROVING DATA PROCESSING SPEED AND EFFICIENCY OF A DATA INPUT AND OUTPUT PIN AND RELATED METHOD FOR CONTROLLING READ AND WRITE	LEE, JUNG-BAE
<u>09633240</u>	<u>6678860</u>	150	08/07/2000	INTEGRATED CIRCUIT MEMORY DEVICES HAVING ERROR CHECKING AND CORRECTION CIRCUITS THEREIN AND METHODS OF OPERATING SAME	LEE, JUNG-BAE
<u>09654148</u>	<u>6477107</u>	150	09/01/2000	INTEGRATED CIRCUIT MEMORY DEVICES HAVING DATA SELECTION CIRCUITS THEREIN WHICH ARE COMPATIBLE WITH SINGLE AND DUAL DATA RATE MODE OPERATION AND METHODS OF OPERATING SAME	LEE, JUNG-BAE
<u>09655643</u>	<u>6564287</u>	150	09/05/2000	SEMICONDUCTOR MEMORY DEVICE HAVING A FIXED CAS LATENCY AND / OR BURST LENGTH	LEE, JUNG-BAE
<u>09667379</u>	<u>6272068</u>	150	09/22/2000	INTEGRATED CIRCUIT MEMORY DEVICES THAT UTILIZE DATA MASKING TECHNIQUES TO FACILITATE TEST MODE ANALYSIS	LEE, JUNG-BAE
<u>09685266</u>	<u>6414517</u>	150	10/10/2000	INPUT BUFFER CIRCUITS WITH INPUT SIGNAL BOOST CAPABILITY AND METHODS OF OPERATION THEREOF	LEE, JUNG-BAE
<u>09721130</u>	<u>6380799</u>	150	11/22/2000	INTERNAL VOLTAGE GENERATION CIRCUIT HAVING STABLE OPERATING CHARACTERISTICS AT LOW EXTERNAL SUPPLY VOLTAGES	LEE, JUNG-BAE
<u>09826566</u>	<u>6466071</u>	150	04/05/2001	METHODS AND CIRCUITS FOR CORRECTING A DUTY-CYCLE OF A SIGNAL	LEE, JUNG-BAE
<u>09834512</u>	<u>6621371</u>	150	04/13/2001	SYSTEM BOARD AND IMPEDANCE CONTROL	LEE, JUNG-BAE

				METHOD THEREOF	
<u>09875364</u>	Not Issued	030	06/05/2001	SIGNAL TRANSMISSION CIRCUIT AND METHOD FOR EQUALIZING DISPARATE DELAY TIMES DYNAMICALLY, AND DATA LATCH CIRCUIT OF SEMICONDUCTOR DEVICE IMPLEMENTING THE SAME	LEE, JUNG-BAE
<u>10054700</u>	<u>6806582</u>	150	01/17/2002	PAD ARRANGEMENT IN SEMICONDUCTOR MEMORY DEVICE AND METHOD OF DRIVING SEMICONDUCTOR DEVICE	LEE, JUNG-BAE
<u>10081546</u>	<u>6728162</u>	150	02/21/2002	DATA INPUT CIRCUIT AND METHOD FOR SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE	LEE, JUNG-BAE
<u>10154734</u>	<u>6636446</u>	150	05/24/2002	SEMICONDUCTOR MEMORY DEVICE HAVING WRITE LATENCY OPERATION AND METHOD THEREOF	LEE, JUNG-BAE
<u>10172314</u>	<u>6747908</u>	150	06/13/2002	SEMICONDUCTOR MEMORY DEVICE AND METHOD OF SELECTING WORD LINE THEREOF	LEE, JUNG-BAE
<u>10205838</u>	<u>6643201</u>	150	07/26/2002	MEMORY DEVICE HAVING READ CHARGE CONTROL, WRITE CHARGE CONTROL AND FLOATING OR PRECHARGE CIRCUITS	LEE, JUNG-BAE
<u>10278071</u>	<u>6819602</u>	150	10/23/2002	MULTIMODE DATA BUFFER AND METHOD FOR CONTROLLING PROPAGATION DELAY TIME	LEE, JUNG-BAE
<u>10281342</u>	<u>6650594</u>	150	10/28/2002	DEVICE AND METHOD FOR SELECTING POWER DOWN EXIT	LEE, JUNG-BAE
<u>10305986</u>	<u>6804163</u>	150	11/29/2002	SEMICONDUCTOR MEMORY DEVICE FOR REDUCING CHIP SIZE	LEE, JUNG-BAE
<u>10453221</u>	<u>6879536</u>	150	06/03/2003	SEMICONDUCTOR MEMORY DEVICE AND SYSTEM OUTPUTTING REFRESH FLAG	LEE, JUNG-BAE
<u>10624783</u>	<u>6826114</u>	150	07/22/2003	DATA PATH RESET CIRCUIT	LEE, JUNG-BAE

				USING CLOCK ENABLE SIGNAL, RESET METHOD, AND SEMICONDUCTOR MEMORY DEVICE INCLUDING THE DATA PATH RESET CIRCUIT AND ADOPTING THE RESET METHOD	
<u>10640146</u>	<u>6826115</u>	150	08/13/2003	CIRCUITS AND METHODS FOR PROVIDING PAGE MODE OPERATION IN SEMICONDUCTOR MEMORY DEVICE HAVING PARTIAL ACTIVATION ARCHITECTURE	LEE, JUNG-BAE
<u>10641637</u>	Not Issued	071	08/14/2003	MEMORY DEVICE HAVING HIGH BUS EFFICIENCY OF NETWORK, OPERATING METHOD OF THE SAME, AND MEMORY SYSTEM INCLUDING THE SAME	LEE, JUNG-BAE
<u>10716120</u>	Not Issued	030	11/18/2003	ON-DIE TERMINATION CIRCUIT AND METHOD FOR REDUCING ON-CHIP DC CURRENT, AND MEMORY SYSTEM INCLUDING MEMORY DEVICE HAVING THE SAME	LEE, JUNG-BAE
<u>10750093</u>	Not Issued	071	12/31/2003	MEMORY SYSTEM MOUNTED DIRECTLY ON BOARD AND ASSOCIATED METHOD	LEE, JUNG-BAE
<u>10771488</u>	Not Issued	041	02/02/2004	DATA INPUT CIRCUIT AND METHOD FOR SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE	LEE, JUNG-BAE
<u>10792425</u>	Not Issued	030	03/03/2004	HIGH BURST RATE WRITE DATA PATHS FOR INTEGRATED CIRCUIT MEMORY DEVICES AND METHODS OF OPERATING SAME	LEE, JUNG-BAE
<u>10797667</u>	Not Issued	030	03/10/2004	SEMICONDUCTOR MEMORY INTEGRATED CIRCUIT	LEE, JUNG-BAE
<u>10798469</u>	Not Issued	030	03/11/2004	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR WRITING AND READING DATA	LEE, JUNG-BAE
<u>10799783</u>	Not	071	03/12/2004	INTERNAL VOLTAGE	LEE, JUNG-BAE

	Issued			GENERATING CIRCUIT FOR SEMICONDUCTOR DEVICE	
<a href="#">10831702</a>	Not Issued	020	04/23/2004	MEMORY MODULE AND METHOD OF TESTING THE SAME	LEE, JUNG-BAE
<a href="#">10886926</a>	Not Issued	030	07/08/2004	MEMORY SYSTEM AND TIMING CONTROL METHOD OF THE SAME	LEE, JUNG-BAE
<a href="#">10895554</a>	Not Issued	030	07/21/2004	PAD ARRANGEMENT IN SEMICONDUCTOR MEMORY DEVICE AND METHOD OF DRIVING SEMICONDUCTOR DEVICE	LEE, JUNG-BAE

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<input type="text" value="LEE"/>	<input type="text" value="JUNG-BAE"/>	<input type="button" value="Search"/>

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**PALM INTRANET**

Day : Sunday  
Date: 5/1/2005  
Time: 09:01:55

**Inventor Name Search Result**

Your Search was:

Last Name = KIM

First Name = KYU-HYOUN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">09521904</a>	<a href="#">6327190</a>	150	03/09/2000	COMPLEMENTARY DIFFERENTIAL INPUT BUFFER FOR A SEMICONDUCTOR MEMORY DEVICE	KIM, KYU-HYOUN
<a href="#">09525730</a>	Not Issued	161	03/14/2000	INPUT CIRCUIT HAVING VOLTAGE GENERATOR SHARED BY MULTIPLE INPUT BUFFERS	KIM, KYU-HYOUN
<a href="#">09685266</a>	<a href="#">6414517</a>	150	10/10/2000	INPUT BUFFER CIRCUITS WITH INPUT SIGNAL BOOST CAPABILITY AND METHODS OF OPERATION THEREOF	KIM, KYU-HYOUN
<a href="#">09713968</a>	<a href="#">6366148</a>	150	11/16/2000	DELAY LOCKED LOOP CIRCUIT AND METHOD FOR GENERATING INTERNAL CLOCK SIGNAL	KIM, KYU-HYOUN
<a href="#">09718158</a>	<a href="#">6359481</a>	150	11/22/2000	DATA SYNCHRONIZATION CIRCUIT	KIM, KYU-HYOUN
<a href="#">09808024</a>	<a href="#">6388485</a>	150	03/15/2001	DELAY-LOCKED LOOP CIRCUIT HAVING MASTER-SLAVE STRUCTURE	KIM, KYU-HYOUN
<a href="#">09816968</a>	<a href="#">6452432</a>	150	03/23/2001	SIGNAL PROCESSING CIRCUITS HAVING A PAIR OF DELAY LOCKED LOOP (DLL) CIRCUITS FOR ADJUSTING A DUTY-CYCLE OF A PERIODIC DIGITAL SIGNAL AND METHODS OF OPERATING SAME	KIM, KYU-HYOUN
<a href="#">09826566</a>	<a href="#">6466071</a>	150	04/05/2001	METHODS AND CIRCUITS FOR CORRECTING A DUTY-CYCLE OF A SIGNAL	KIM, KYU-HYOUN
<a href="#">09850019</a>	<a href="#">6459314</a>	150	05/07/2001	DELAY LOCKED LOOP CIRCUIT HAVING DUTY	KIM, KYU-HYOUN

				CYCLE CORRECTION FUNCTION AND DELAY LOCKING METHOD	
<u>09861954</u>	<u>6535051</u>	150	05/21/2001	CHARGE PUMP CIRCUIT	KIM, KYU- HYOUN
<u>09875364</u>	Not Issued	030	06/05/2001	SIGNAL TRANSMISSION CIRCUIT AND METHOD FOR EQUALIZING DISPARATE DELAY TIMES DYNAMICALLY, AND DATA LATCH CIRCUIT OF SEMICONDUCTOR DEVICE IMPLEMENTING THE SAME	KIM, KYU- HYOUN
<u>09935096</u>	<u>6486719</u>	150	08/22/2001	FLIP-FLOP CIRCUITS HAVING DIGITAL-TO-TIME CONVERSION LATCHES THEREIN	KIM, KYU- HYOUN
<u>10101475</u>	<u>6590421</u>	150	03/19/2002	SEMICONDUCTOR DEVICE AND METHOD OF OUTPUTTING DATA THEREIN	KIM, KYU- HYOUN
<u>10108671</u>	<u>6693842</u>	150	03/28/2002	SEMICONDUCTOR DEVICE HAVING A PLURALITY OF OUTPUT SIGNALS	KIM, KYU- HYOUN
<u>10112108</u>	<u>6639868</u>	150	03/28/2002	SDRAM HAVING DATA LATCH CIRCUIT FOR OUTPUTTING INPUT DATA IN SYNCHRONIZATION WITH A PLURALITY OF CONTROL SIGNALS	KIM, KYU- HYOUN
<u>10160703</u>	<u>6704228</u>	150	05/30/2002	SEMICONDUCTOR MEMORY DEVICE POST-REPAIR CIRCUIT AND METHOD	KIM, KYU- HYOUN
<u>10191413</u>	<u>6590434</u>	150	07/10/2002	DELAY TIME CONTROLLING CIRCUIT AND METHOD FOR CONTROLLING DELAY TIME	KIM, KYU- HYOUN
<u>10340831</u>	<u>6734707</u>	150	01/13/2003	DATA INPUT CIRCUIT FOR REDUCING LOADING DIFFERENCE BETWEEN FETCH SIGNAL AND MULTIPLE DATA IN SEMICONDUCTOR DEVICE	KIM, KYU- HYOUN
<u>10405484</u>	<u>6853317</u>	150	04/03/2003	CIRCUIT AND METHOD FOR GENERATING MODE REGISTER SET CODE	KIM, KYU- HYOUN
<u>10611255</u>	<u>6847559</u>	150	07/01/2003	INPUT BUFFER CIRCUIT OF A SYNCHRONOUS	KIM, KYU- HYOUN

				SEMICONDUCTOR MEMORY DEVICE	
<u>10619821</u>	Not Issued	030	07/14/2003	DELAY LOCKED LOOP CIRCUIT FOR INTERNALLY CORRECTING DUTY CYCLE AND DUTY CYCLE CORRECTION METHOD THEREOF	KIM, KYU-HYOUN
<u>10631412</u>	Not Issued	041	07/30/2003	OUTPUT DRIVER CAPABLE OF CONTROLLING SLEW RATE OF OUTPUT SIGNAL ACCORDING TO OPERATING FREQUENCY INFORMATION OR CAS LATENCY INFORMATION	KIM, KYU-HYOUN
<u>10631414</u>	<u>6870776</u>	150	07/30/2003	DATA OUTPUT CIRCUIT IN COMBINED SDR/DDR SEMICONDUCTOR MEMORY DEVICE	KIM, KYU-HYOUN
<u>10645018</u>	Not Issued	071	08/21/2003	SEMICONDUCTOR MEMORY DEVICE HAVING PARTIALLY CONTROLLED DELAY LOCKED LOOP	KIM, KYU-HYOUN
<u>10656303</u>	Not Issued	092	09/04/2003	SEMICONDUCTOR MEMORY DEVICE HAVING DUTY CYCLE CORRECTION CIRCUIT AND INTERPOLATION CIRCUIT INTERPOLATING CLOCK SIGNAL IN THE SEMICONDUCTOR MEMORY DEVICE	KIM, KYU-HYOUN
<u>10671105</u>	Not Issued	071	09/25/2003	SEMICONDUCTOR DEVICE COMPRISING FREQUENCY MULTIPLIER OF EXTERNAL CLOCK AND OUTPUT BUFFER OF TEST DATA AND SEMICONDUCTOR TEST METHOD	KIM, KYU-HYOUN
<u>10672461</u>	Not Issued	030	09/26/2003	SYNCHRONOUS SEMICONDUCTOR DEVICE AND METHOD OF PREVENTING COUPLING BETWEEN DATA BUSES	KIM, KYU-HYOUN
<u>10716146</u>	Not Issued	071	11/18/2003	TIME DELAY COMPENSATION CIRCUIT COMPRISING DELAY CELLS HAVING VARIOUS UNIT TIME DELAYS	KIM, KYU-HYOUN

<u>10774933</u>	Not Issued	030	02/09/2004	DELAY-LOCKED LOOP (DLL) CAPABLE OF DIRECTLY RECEIVING EXTERNAL CLOCK SIGNALS	KIM, KYU-HYOUN
<u>10793001</u>	Not Issued	030	03/04/2004	INTEGRATED CIRCUIT DEVICES HAVING IMPROVED DUTY CYCLE CORRECTION AND METHODS OF OPERATING THE SAME	KIM, KYU-HYOUN
<u>10793209</u>	Not Issued	030	03/04/2004	DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY SEMICONDUCTOR DEVICE	KIM, KYU-HYOUN
<u>10799783</u>	Not Issued	071	03/12/2004	INTERNAL VOLTAGE GENERATING CIRCUIT FOR SEMICONDUCTOR DEVICE	KIM, KYU-HYOUN
<u>10837391</u>	Not Issued	030	04/29/2004	SPREAD SPECTRUM CLOCK GENERATOR	KIM, KYU-HYOUN
<u>10841866</u>	Not Issued	030	05/06/2004	HYPER-RING OSCILLATOR	KIM, KYU-HYOUN
<u>10884723</u>	Not Issued	030	07/02/2004	BUFFER CIRCUIT AND MEMORY SYSTEM FOR SELECTIVELY OUTPUTTING DATA STROBE SIGNAL ACCORDING TO NUMBER OF DATA BITS	KIM, KYU-HYOUN
<u>10890493</u>	Not Issued	030	07/13/2004	INTERFACE CIRCUIT AND SIGNAL CLAMPING CIRCUIT USING LEVEL-DOWN SHIFTER	KIM, KYU-HYOUN
<u>10925522</u>	Not Issued	030	08/25/2004	JITTER SUPPRESSING DELAY LOCKED LOOP CIRCUITS AND RELATED METHODS	KIM, KYU-HYOUN
<u>10949165</u>	Not Issued	030	09/24/2004	INPUT BUFFER CAPABLE OF REDUCING INPUT CAPACITANCE SEEN BY INPUT SIGNAL	KIM, KYU-HYOUN
<u>10990412</u>	Not Issued	030	11/18/2004	INPUT BUFFER FOR DETECTING AN INPUT SIGNAL	KIM, KYU-HYOUN
<u>11005821</u>	Not Issued	030	12/07/2004	DUTY CYCLE CORRECTION CIRCUITS SUITABLE FOR USE IN DELAY-LOCKED LOOPS AND METHODS OF CORRECTING DUTY CYCLES OF PERIODIC SIGNALS	KIM, KYU-HYOUN

## Inventor Search Completed: No Records to Display.

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